

REMARKS

Claims 1, 3, 5, 6, 8 – 19, 22, 24, 25, and 27 – 39 are pending in this application. Claims 40 is canceled. Claims 38 and 39 are indicated to be allowable. Claims 1, 3, 5, 8 – 19, 22, 24, and 27 – 37 are indicated to be directed to allowable subject matter pending correction of certain informalities. The amendments presented above follow the examiner's suggestions with one exception, and thus, these claims should also be allowable. The exception is Claim 36, where it is believed that the necessary antecedent basis for "Inter-Symbol Interference" in line 14 is present in lines 12 and 13. No new matter is being added.

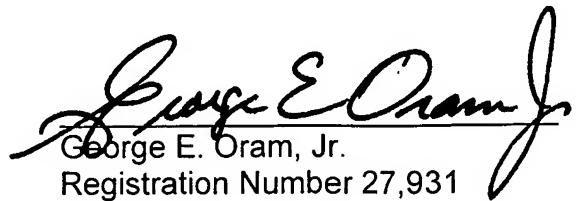
Claims 6 and 25 were previously rejected under 35 U.S.C. § 112, second paragraph, as being misdescriptive and indefinite. Contrary to the Office Action, the features of Claims 6 and 25 that the gate width of the third transistor is smaller than a gate width of the fourth transistor is clearly supported in the Specification in at least the material of lines 2 – 7 and 26 – 29 on page 14. Figures 8, 9, and 13 – 17 are mere circuit diagrams which do not indicate gate widths of transistors 3 and 30 (30 and 30'). It is respectfully submitted that these claims are sufficiently supported and are not indefinite. Withdrawal of the rejection is requested.

In view of all of the above, it is believed that all of Claims 1, 3, 5, 6, 8 – 19, 22, 24, 25, and 27 – 39 are allowable. An early Notice of Allowance is requested.

In the event that this paper is not considered to be timely filed, an appropriate extension of time is requested. Any fees for such an extension, together with any

additional fees that may be due with respect to this paper, may be charged to Deposit Account No. 01-2300, referencing Attorney Docket Number 100021-00069.

Respectfully submitted,



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